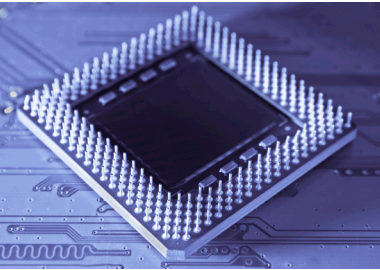


ESL design automation solutions that work for your business

UNLEASH THE POWER OF YOUR EMBEDDED SYSTEMS APPLICATIONS



ESLERATE

Making fast *faster*.

Drive out cost, complexity, and development time with *ESLerate™*, the industry's only electronic system-level (ESL) design automation tool for SoC FPGA platforms that provides a comprehensive solution for today's embedded systems developers to achieve optimal performance, minimize cost, and reduce design times from *months to hours*.



Features and Benefits

- Supports high-level synthesis of software binary and assembly code into RTL VHDL and Verilog hardware models
- Automated hardware-software interface synthesis
- Automated testbench generation for bit-true verification
- Achieve optimal performance through innovative optimizations and automated streaming architectures
- Quickly explore hardware-software trade-offs
- Migrate legacy assembly code to newer FPGA platforms
- Easily integrated with industry-standard design tools
- Reduce FPGA design time from months to hours
- Meet performance, cost, and time-to-market constraints

Today's ESL design automation tool industry consists of a variety of design flow methods. Many of these tools require users to rewrite their software algorithms in specific languages, modify their development process, or integrate costly third-party tools. These requirements often impact development times and budget constraints.

ESLerate is the industry's only high-level synthesis solution that provides a path for translating binary and assembly code for general-purpose embedded processors into powerful, tightly-coupled RTL hardware accelerators for SoC FPGA platforms. Whether you are developing a software application in C, C++, assembly, or a combination thereof, software binaries represent a unified description of the algorithm. The unique characteristics of the binary code are utilized in optimizing design performance, area, and power for real-time embedded applications, while decreasing design costs and reducing development time from *months to hours*.

ESLerate accelerates embedded software applications by partitioning the software binaries into separate software and hardware components, which have been optimized for performance. The tool generates the necessary hardware and software communication interfaces, and reconstructs the binary executable with appropriate instructions to communicate with the hardware accelerator. *ESLerate* incorporates advanced optimizations such as automatic streaming architectures, hardware pipelining, low-power optimizations, and smart scheduling. It supports translation of hand-coded assembly, third-party libraries, and legacy code from general-purpose processors to FPGA platforms. The tool is easily integrated within industry-standard FPGA development suites, and supports all Xilinx, Altera, and Actel SoC FPGA platforms.



BINACHIP

www.binachip.com/eslerate

Integrated Embedded SoC Development Environment

ESL DESIGN AUTOMATION

Meet your design goals, reduce development time, and cut cost through ESL design automation by raising the level of abstraction for electronic design models to high-level software languages.

TURNKEY SOLUTIONS

Quickly explore hardware-software trade-offs, modify and optimize design parameters in high-level source code, or automatically retarget design to different FPGA platforms on the fly.

KNOWLEDGE BASE

Software and product updates, documentation, webinars, white-papers, and tutorials with real-world design examples are available online for download.

FLEXIBLE LICENSING

Node-locked and floating network licensing models are available for purchase, or request a limited demo evaluation license.

TECHNICAL SUPPORT

Work directly with our support engineers who are readily available to solve any technical problems and provide quick-response support by email, phone, and online webcase.

SYSTEM REQUIREMENTS

OS: Windows 2000 / NT / XP / 7

Architecture: 32-bit and 64-bit

Xilinx Users: ISE Design Suite

Altera Users: Quartus II

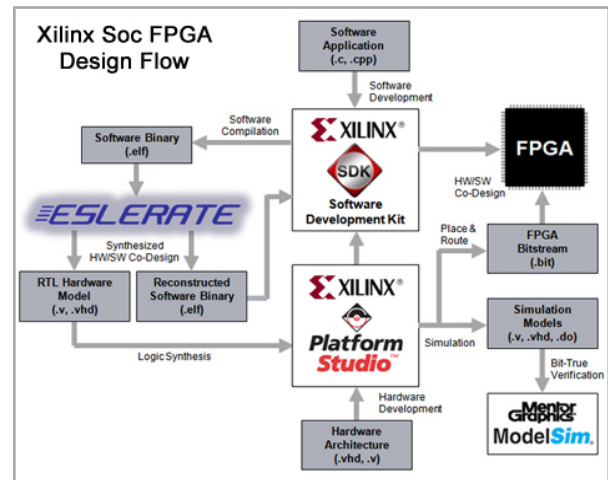
Actel Users: Libero IDE

ESLerate supports the SoC FPGA platforms, embedded processors, and development tool suites from Xilinx, Altera, and Actel. While the development tools vary between FPGA manufactures, the SoC design process remains very similar for all three platforms.

For example, in a typical Xilinx SoC design process, a system architecture consisting of processors, memory, peripherals, and custom IP modules is first developed in Xilinx Platform Studio. The complete hardware architecture model is then imported into the Xilinx Software Development Kit (SDK), where a software application is developed and compiled for an embedded processor, such as PowerPC or MicroBlaze. The resulting software application may then be profiled to determine which functions in the design should be accelerated in custom logic.

High-level synthesis of the software application is performed by importing the binary executable into ESLerate. The tool performs hardware-software partitioning of the application by generating an optimized RTL model of the software functions and reconstructing the executable with the necessary instructions to communicate with the hardware. The RTL model is imported as an IP core into the Platform Studio project. Simulation of the complete SoC design, along with the reconstructed binary is performed using Mentor Graphics ModelSim. Once the bit-true verification of the system is completed, the design is again synthesized, mapped, and routed with Platform Studio, which generates a programmable bit stream for the target Xilinx SoC FPGA.

Supported SoC FPGA Platforms				
FPGA Manufacturer	Development Tool	SoC FPGA Platform	Embedded Processor	Bus Interface
Xilinx	ISE Design Suite	Virtex 2P / 4 / 5 / 6 Spartan 2E / 3E / 6	ARM Cortex-A9 MicroBlaze PowerPC 404 / 440	CoreConnect
Altera	Quartus II	Cyclone II / III Stratix II / III / IV	Nios II ARM Cortex-M1	Avalon
Actel	Libero IDE	Fusion IGLOO ProASIC3 / 3L	Nios II ARM Cortex-M1	AMBA



unleash the power of your
embedded systems applications

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